REMARKS

In the Office Action, Claims 1-24 are pending, were examined and stand rejected. In this Response, Claims 1, 11, 16 and 21 are amended, Claim 19 is cancelled and no claims are added. Applicants respectfully request reconsideration of pending Claims 1-18 and 20-24 in view of the following remarks.

I. Double Patenting Rejection

The Examiner rejects Applicants' invention under the provisional obviousness-type double patenting rejection as not patentably distinct from the claimed inventions of co-pending U.S. Patent Application No. 10/781,512 although the conflicting claims are not identical. Applicants hold in abeyance this rejection until such time as the claims on which the rejection is premised are granted.

II. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 1-24 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,158,018 to Bernasconi et al. ("Bernasconi") in view of U.S. Patent No. 5,966,547 to Hagan et al. ("Hagan"). Applicants respectfully traverse this rejection.

Regarding Claim 1, Claim 1 is amended to recite the following claim feature, which is neither taught nor suggested by the prior art combination of Bernasconi in view of Hagan:

> a patch module coupled to the completion queue, the patch module to capture an incoming request cycle received by the I/O controller and to determine if the captured incoming request cycle matches one or more of preprogrammed trigger conditions, wherein the patch module can work around a captured non-posted request cycle by controlling header information loaded into the completion queue and by instructing the completion queue whether or not to discard a completion packed received from a designated end-device. (Emphasis added.)

According to the Examiner:

> Bernasconi discloses a system comprising: an input/output (I/O) controller (controller 14, fig. 1) to receive request cycles from a request device (16, fig. 1); and a patch module (patching circuitry 22, fig. 1), the patch module to capture an incoming cycle (24, fig. 1) received by the I/O controller and to determine if the captured incoming cycle matches one or more of preprogrammed trigger conditions. (pg. 3, ¶2 of the Office Action mailed April 21, 2006.)

As indicated by the cited passage above, the Examiner asserts FIG. 1 of Bernasconi discloses a patch module that captures an incoming cycle, as recited by amended Claim 1. Applicant respectfully disagrees with the Examiner. As taught by Bernasconi:

> Again with respect to FIG. 1, a bus 24 provides the current DSP program address from the embedded DSP 16 (hereafter more simply referred to as "DS") to the patching circuitry 22, the ROM 18, and the RAM 20. Additionally, DSP program software stored in the ROM 18 is provided via bus 26, the patching circuitry 22, and bus 30 to the DSP 16. Similarly, corrected DSP program software stored in the ROM 18 is provided via bus 26, the patching circuitry 22, and bus 30 to the DSP 16. Similarly, corrected DSP program software stored in the RAM 20 such as section 20b of the RAM 20 is provided via bus 28, the patching circuitry 22, and bus 30 to the DSP 16. (col. 6, lines 15-23.) (Emphasis added.)

As indicated by the cited passage above, reference numeral "24" of FIG. 1 refers to a bus, which as taught by Bernasconi, provides the current DSP program address from the embedded DSP 16 to the patching circuitry 22, the ROM 18 and the RAM 20. (*See*, supra.) As further disclosed by Bernasconi, the DSP program address is compared against a break address to identify flawed DSP program software. (*See*, col. 9, lines 53-57.)

Applicant respectfully submits that the use current DSP program address provided by bus 24 from DSP 16 to patching circuitry 22, ROM 18 and RAM 20 to identify flawed DP program software neither teaches nor suggests the capture of an incoming request cycle received by an I/O controller, as recited by amended Claim 1.

Regarding the term "request cycles," Applicant's specification describes two categories of such request cycles, including a write request cycle that is used to transport data from a host processor to an end-user device or a read request cycle that is used to read data from the end-user device. (*See*, pg. 1, ¶3 of Applicant's specification.) Applicant respectfully submits that current DSP program addresses provided by bus 24 neither teach nor suggest the incoming request cycles referred to by amended Claim 1.

As mandated by case law, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). All words in a claim must be considered in judging the patentability of that claim against the prior art. In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (C.C.P.A. 1970.)

Here, Applicant respectfully submits that the Examiner has failed to consider the term "request cycle" as well as the term "completion," as recited by amended Claim 1. To further clarify the language of Claim 1, the term "packet" is added to amended Claim 1, such that amended Claim 1 recites:

> instructing the completion queue whether or not to discard a completion packet received from a designated end-device. (Emphasis added.)

According the Examiner:

> In regards to "a completion received from a designated end-device being discard". Once an incoming cycle (24), received from a requesting device, such as (16), which can also be an end-device, it is considered complete until an error or a fault is found in it; as it go through the patch circuitry 22, it will be discard because of the error or the fault. Therefore, this limitation is inherently met. (pg. 3, ¶2 of the Office Action mailed April 21, 2006.)

The completion packet received from the designated end-device, as recited by amended Claim 1, as known to those skilled in the art, refers to a packet which is transmitted from a target device to a requesting device to indicate that the request cycle has been successfully completed. (*See*, Applicant's specification, supra.) Conversely, the discarding of a current DSP program address received by patch circuitry 22 via bus 24 does not inherently meet "a completion received from a designated end-device being discard," as referred to by the Examiner. (*See*, supra.) As mandated by case law:

> In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teaching of the applied prior art. Ex Parte Levy, 17 USPQ 2d 1461, 1464 (Bd. Pat. App. & Intr. 1990.) (Emphasis added.)

Applicant respectfully submits that the processing of a current DSP program address by patch circuitry, as taught by Bernasconi, and the eventually discarding of the DSP program address by patch circuitry 22, as indicated by the Examiner, fails to provide a basis in fact under technical reasoning that the discarding of a completion received from a designated end device necessarily flows from the teachings of Bernasconi. Applicant respectfully submits that the instructing of the completion queue on whether or not to discard a completion packet received from a designated end-device, as recited by amended Claim 1, is not inherently disclosed by Bernasconi. Id.

As correctly noted by the Examiner:

> Bernasconi fails to specifically teach specifying whether the I/O controller including a patch module (patching circuitry 22) coupled to a completion queue is to be loaded with information from non-posted cycle. (pg. 3, ¶3 of the Office Action mailed April 21, 2006.)

As a result, the Examiner cites Hagan. Regarding the Examiner's citing of Hagan, Applicant respectfully submits that Hagan fails to provide any teachings or suggestions with regard to the non-posted request cycles referred to by amended Claim 1. Applicant has defined the term "non-posted request cycles" and "non-posted cycle" as referring to any request cycle that requires completion including, but not limited to, memory requests, configuration read requests and configuration write requests. (*See*, pg. 4, ¶0016, lines 10-14 of Applicant's specification.)

Conversely, Hagan, is directed to a method and process for posting events or tasks to a shared queue and a multi-processor data processing system to post events or tasks to another processor to perform. (*See*, col. 1, lines 10-17.) Applicant respectfully submits that the communication between such processors to post events or tasks to another processor to perform provide no teachings or suggestions with regards to non-posted request cycles, as referred to by amended Claim 1.

Accordingly, for at least the reasons provided above, Applicant respectfully submits that the Examiner has failed to establish a *prima facie* case of obviousness of amended Claim 1, since all claim limitations recited by amended Claim 1 are neither taught nor suggested by the prior art combination of Bernasconi in view of Hagan. In re Royka, supra.

Consequently, Applicant respectfully submits that Claim 1, as amended, is patentable over the combination of Bernasconi in view of Hagan, as well as the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of amended Claim 1.

Regarding Claims 2-9, Claims 2-9, based on their dependency from Claim 1, are also patentable over the combination of Bernasconi in view of Hagan. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 2-9.

Regarding Claims 11 and 21, Claims 11 and 21 are amended to recite the following claim feature, which is neither taught nor suggested by the prior art combination of Bernasconi in view of Hagan:

> instructing the completion queue whether or not to discard a completion packet received from a designated end-device. (Emphasis added.)

Applicant respectfully submits that the above-recited feature of amended Claims 11 and 21 are analogous to the previously-described feature of amended Claim 1. For at least the reasons indicated above, Applicant respectfully submits that the prior art combination of Bernasconi in view of Hagan fails to provide any teachings or suggestions regarding instructing completion queue whether or not to discard a completion packet received from a designated end-device, as recited by amended Claim 11.

Furthermore, Applicant respectfully submits that the prior art combination of Bernasconi in view of Hagan fails to provide any teaching or suggestion with regards to the non-posted request cycle, referred to by amended Claim 11. Consequently, Applicant respectfully submits that the Examiner is prohibited from establishing a *prima facie* case of obviousness of amended Claims 11 and 21, since all limitations recited by amended Claims 11 and 21 are neither taught nor suggested by the prior art combination of Bernasconi in view of Hagan. Id.

Accordingly, for at least the reasons provided above, Applicant respectfully submits that Claims 11 and 21, as amended, are patentable over the prior art combination of Bernasconi in view of Hagan. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of amended Claims 11 and 21.

Regarding Claims 12-15 and 22-24, Claims 12-15 and 22-24, based on their dependency from Claims 11 and 21, respectively, are also patentable over the prior art combination of Bernasconi in view of Hagan. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 12-15 and 22-24.

Regarding Claim 16, Claim 16, as amended, recites the following claim features, which are neither taught nor suggested by the prior art combination of Bernasconi in view of Hagan:

> a control logic coupled to the trigger-matching logic to select a set of instructions upon detection of at least one matched trigger condition and to execute operations as specified by the selected set of instructions, wherein if the captured cycle that caused a trigger is a non-posted cycle, the control logic instructs a completion queue to load the completion queue with one of the

following (1) unmodified header information from the captured non-posted cycle, (2) modified header information associated with modified non-posted cycle, or (3) header information associated with a new cycle generated in response the captured cycle,

wherein the control logic instructs the completion queue whether or not to return a completion packet associated with the modified non-posted cycle to the requesting device. (Emphasis added.)

As indicated by the above-recited feature of amended Claim 16, the above-recited feature of amended Claim 16 recites an analogous claim feature to amended Claim 1:

wherein the control logic instructs the completion queue whether or not to return a completion packet associated with the modified non-posted cycle to the requesting device. (Emphasis added.)

Accordingly, Applicant's arguments provided above with regard to the §103(a) rejection of amended Claim 1, as unpatentable over the prior art combination of Bernasconi in view of Hagan, equally apply to the §103(a) rejection of Claim 16 as unpatentable over such references. Hence, for at least the reasons provided above, Applicant respectfully submits that Applicant's amendment to Claim 16 prohibits the Examiner from establishing a *prima facie* case of obviousness of amended Claim 16, since all claim limitations recited by amended Claim 16 are neither taught nor suggested by the prior art combination of Bernasconi in view of Hagan. Id.

Therefore, for at least the reasons provided above, Applicant respectfully submits that Claim 16, as amended, is patentable over the prior combination of Bernasconi in view of Hagan. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of amended Claim 16.

Regarding Claims 17, 18 and 20, Claims 17, 18 and 20, based on their dependency from Claim 16, are also patentable over the prior art combination of Bernasconi in view of Hagan. Therefore, for at least the reasons provided above, Applicant respectfully submits that Claims 17, 18 and 20, as amended, are patentable over the prior combination of Bernasconi in view of Hagan. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 17, 18 and 20.

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In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: July 21, 2006

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I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Marilyn Bass July 21, 2006